In the Claims

Claims 1-24 are canceled.

Cancel claims 25-30.

Claims 31-37 are canceled.

Cancel claims 38-49.

50. [Original] A process for reading data from a SRAM cell including a first transistor of a first conductivity type and a second transistor of a second conductivity type comprising:

increasing a voltage across a portion of the cell including two power electrodes of one of the first and second transistors; and

monitoring a current through the power electrodes of the one transistor.

51. [Original] The process of claim 50, wherein increasing comprises increasing the voltage by less than an amount represented by a turn-on voltage of the one transistor.

52. [Original] The process of claim 50, wherein the first transistor comprises an ultrathin PMOS transistor and the second transistor comprises an ultrathin NMOS transistor, and wherein:

increasing comprises lowering a voltage impressed on a source of the NMOS transistor below a ground reference voltage; and

monitoring comprises monitoring a drain current of the NMOS transistor.

53. [Original] The process of claim 50, further comprising:

determining that a first logical state was stored in the SRAM cell when no current increase accompanies increasing; and

determining that a second logical state different than the first logical state was stored in the SRAM cell when a current increase accompanies increasing.

54. [Original] The process of claim 50, wherein the first transistor comprises an ultrathin PMOS transistor having a gate, a source and a drain and the second transistor comprises an ultrathin NMOS transistor having a gate, a source and a drain, the NMOS transistor source being coupled to a row address line and the NMOS transistor drain being coupled to a column address line and wherein:

increasing comprises reducing a potential applied to the row address line; and

monitoring comprises monitoring a current through the column address line.

55. [Original] The process of claim 50, wherein the first transistor comprises an ultrathin PMOS transistor having a gate, a source and a drain and the second transistor comprises an ultrathin NMOS transistor having a gate, a source and a drain and wherein increasing comprises increasing a gate-source voltage of the NMOS transistor to a value that is less than a threshold voltage of the NMOS transistor.